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MECHATRONICS LABS SRL

IO-LINK SLAVE MODULE IOLS-E

I IO-Link Slave Module is a family of solutions for integrating the **IO-Link** interface quickly.
IO-Link Slave Module family have the following advantageous features:

IO-Link

- Single component for bilateral transfer of data
- The communication IO-Link Stack is integrated. Does not need of additional developments firmware for the management of the Stack.
- IO-Link references to IO-Link Interface and System Specification Version 1.1
- Application for the management of analog sensors and digital IO on Shift Register, already integrated Shift Register
- SSIO for Serial Shift Register IN and OUT data rate up to 5Mbit / sec with minimum cycle time 250 us
- General purpose I/Os configurable
- Modbus RTU host configuration
- SSIO or SPI host configuration
- Develop your custom application inside and use our library stack features.
- Dimensions: 12,7 x 9 mm
- Host data transfer rates up to 5Mbit / sec in SPI communication and up to 512Kbit / sec in RTU Modbus communication
- Analog INPUT whit ADC 12bits
- Analog OUTPUT with DAC 10bits
- Sampling up to 100Ksample / s
- Configuration via Hardware
- External components only: IO-Link connector and signal LEDs of the communication status (optional).
- Also available in Tape and Reel
- IO-Link stack Royalties Free
- Power 3.3 VDC

INDEX

1 TYPICAL APPLICATIONS

- Sensors and actuators products.
- IoT and Industry 4.0 products.
- Automation components.

1.1 Ordering information and packaging

Type number	Package	Package style	Package MOQ
IOLS-E-00S-R	uModule25	Reel	1000
IOLS-E-00S-T	uModule25	Tape and Cut	1
IOLS-E-00S-E	uModule25	Re-Reel	500

The IOLS-E packages typically have the following top-side marking:

IOLS-E-00S
Rnnnnnn
yyww

Rnnnnnn= product revision and serial number
yyww= year and weeks of the product was manufactured

2 BLOCK DIAGRAM IOLS-E

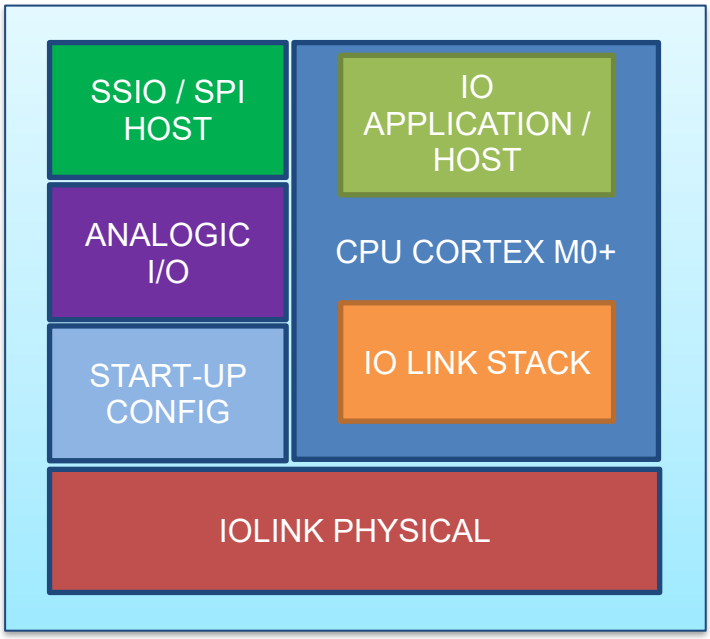


Figure 2.1 IOLS-E-00S Synthetic Block Diagram

For descriptions of each function, refer to section 4.

3 DEVICE PIN OUT AND SIGNAL DESCRIPTION

3.1 Package

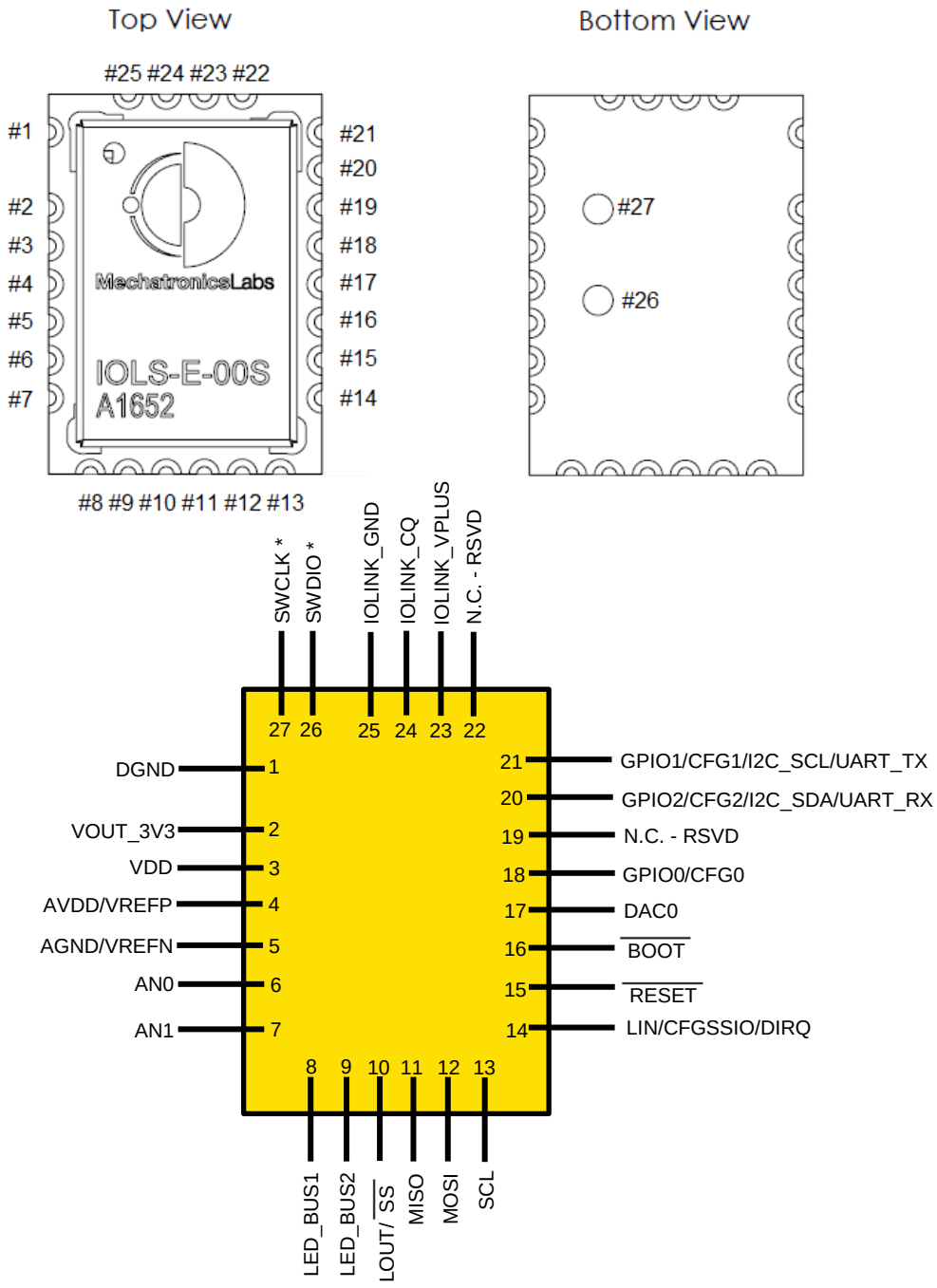


Figure 3.1 Package Pin Out uModule25

*** Note**: Use these pins only if the module IOLS-E is used in Application mode. These pins are used for debug. Refer to specific chapter for details (4.8 - Application mode feature).

3.2 Pin Out Description

Pin	Name	Type	Description
25	IOLINK_GND	PWR	Ground IO-Link
24	IOLINK_CQ	ANA IO	IO-Link data signal
23	IOLINK_VPLUS	PWR	IO-Link supply voltage
8	LED_BUS1	CO	Bus status OK
9	LED_BUS2	CO	Bus status Fault

Table 3.2.1 Interface IO-Link Group

Pin	Name	Type	Description
1	DGND	PWR	Device ground supply
2	VOUT_3V3	PWR	Output supply, limited to 50mA current load. Offers sensor and application power supply.
3	VDD	PWR	Supply voltage for the I/O pad ring, the core voltage regulator, and the analog peripherals.
4	AVDD/VREFP	PWR	ADC positive reference voltage. Must be equal or lower than VDD. Should be tied to VDD if the ADC and DAC are not used.
5	AGND/VREFN	PWR	ADC negative reference voltage. Analog ground supply.

Table 3.2.2 Power and Ground Group

Pin	Name	Type	Description
6	AN0	ANA I	Analog Input signal 0 – Direct to ADC input without conditional signal circuit
7	AN1	ANA I	Analog Input signal 1 – Direct to ADC input without conditional signal circuit
17	DAC0	ANA O	Analog Output signal 0 – Direct from DAC output of internal peripheral, without conditional signal circuit.

10	LOUT	CO	Latch Output Data when use in SSIO mode configuration. Typically this pin work for shift register set output.
	$\overline{SS}$	CI	Select slave Input when use in HOST mode configuration with interface SPI. Module is a slave peripheral on SPI bus.
14	LIN	CO	Latch Input Data when use in SSIO mode configuration. Typically this pin work for shift register load input.
	DIRQ	CO	Output signal, Data Interrupt Request. When module is in HOST mode configuration, this pin can be used for synchronize host to IO-Link cycle data process exchange.
	CFGSSIO	CI	Digital Input for only start-up configuration. With external pull-up: HOST mode configuration Without external pull-up: SSIO mode configuration
11	MISO	CI/CO	In SSIO mode configuration is SDI signal, for read data input from shift register. In HOST mode configuration is a MISO signal of SPI bus, Slave Output signal. Module is a slave peripheral on SPI bus.
12	MOSI	CO/CI	In SSIO mode configuration is SDO signal, for write data output to shift register. In HOST mode configuration is a MOSI signal of SPI bus, Slave Input signal. Module is a slave peripheral on SPI bus.
13	SCLK	CO/CI	In SSIO mode configuration is a serial clock output signal for shift register communication. In HOST mode configuration is a serial clock input signal used from a master on SPI bus. Module is a slave peripheral on SPI bus.
15	$\overline{RESET}$	CI	Active low reset pin.
16	$\overline{BOOT}$	CI	A LOW level on this pin during reset start the BOOT handler, for firmware update by UART.

19,22	N.C. - RSVD	NC	Attention: this pin have internal connection but is reserved to future improved. Not connect. [1]

Table 3.2.3 IN/OUT and reserved Group

n.Pin	Name	Type	Description
18	GPIO0	CI/CO	General purpose 0 Input/Output function.
	CFG0	CI	Digital Input 0 for only start-up configuration. Used with pull-up or pull-down external for some start-up settings.
21	GPIO1	CI/CO	General purpose 1 Input/Output function.
	CFG1	CI	Digital Input 1 for only start-up configuration. Used with pull-up or pull-down external for some start-up settings.
	I2C_SCL	CI/CO	I^2C communication bus for diagnostic. Interface signal clock. Module is a slave I^2C peripheral.
	UART_TX	CO	Asynchronous Serial communication TX signal, used in HOST mode configuration for Modbus RTU interface in alternative to SPI.
20	GPIO2	CI/CO	General purpose 2 Input/Output function.
	CFG2	CI	Digital Input 2 for only start-up configuration. Used with pull-up or pull-down external for some start-up settings.
	I2C_SDA	CI/CO	I^2C communication bus for diagnostic. Interface bidirectional data. Module is a slave I^2C peripheral.
	UART_RX	CI	Asynchronous Serial communication RX signal, used in HOST mode configuration for Modbus RTU interface in alternative to SPI.

Table 3.2.4 General purpose I/O and UART Interface

Pin	Name	Type	Description
26	SWDIO	CI/CO	Serial Wire Debug I/O. Note: This pin is used only in APPLICATION mode. Refer to chapter 4.8
27	SWCLK	CI	Serial Wire Clock Note: This pin is used only in APPLICATION mode. Refer to chapter 4.8

Table 3.2.5 Special function

Note:

1- Do not connect.
2- Pin type: PWR: power, CI: CMOS input, CO: CMOS output, ANA IO: Analogue input output, ANA O: Analogue output, NC: Not Connected.

4 FUNCTIONAL DESCRIPTION

The **IOLS-E** is an embedded component that facilitates the integration of IO-Link devices that need to communicate on the IO-Link protocol.
The component is designed to be configured without the need to use additional microprocessors, and / or firmware integrations.
The **IO-Link Slave Module** is equipped of the application for the management of analog sensors and digital I/O on Shift Register and IO-Link communication stack.
It was designed to be embedded directly in the hardware of the sensor as a single component already been programmed.
It is equipped with host communication in SPI or UART Modbus interface.

4.1 Functional Block

The paragraphs below describe in detail each function within the IOL-E-01S. Please refer to the block diagram shown in Figure 4.1.

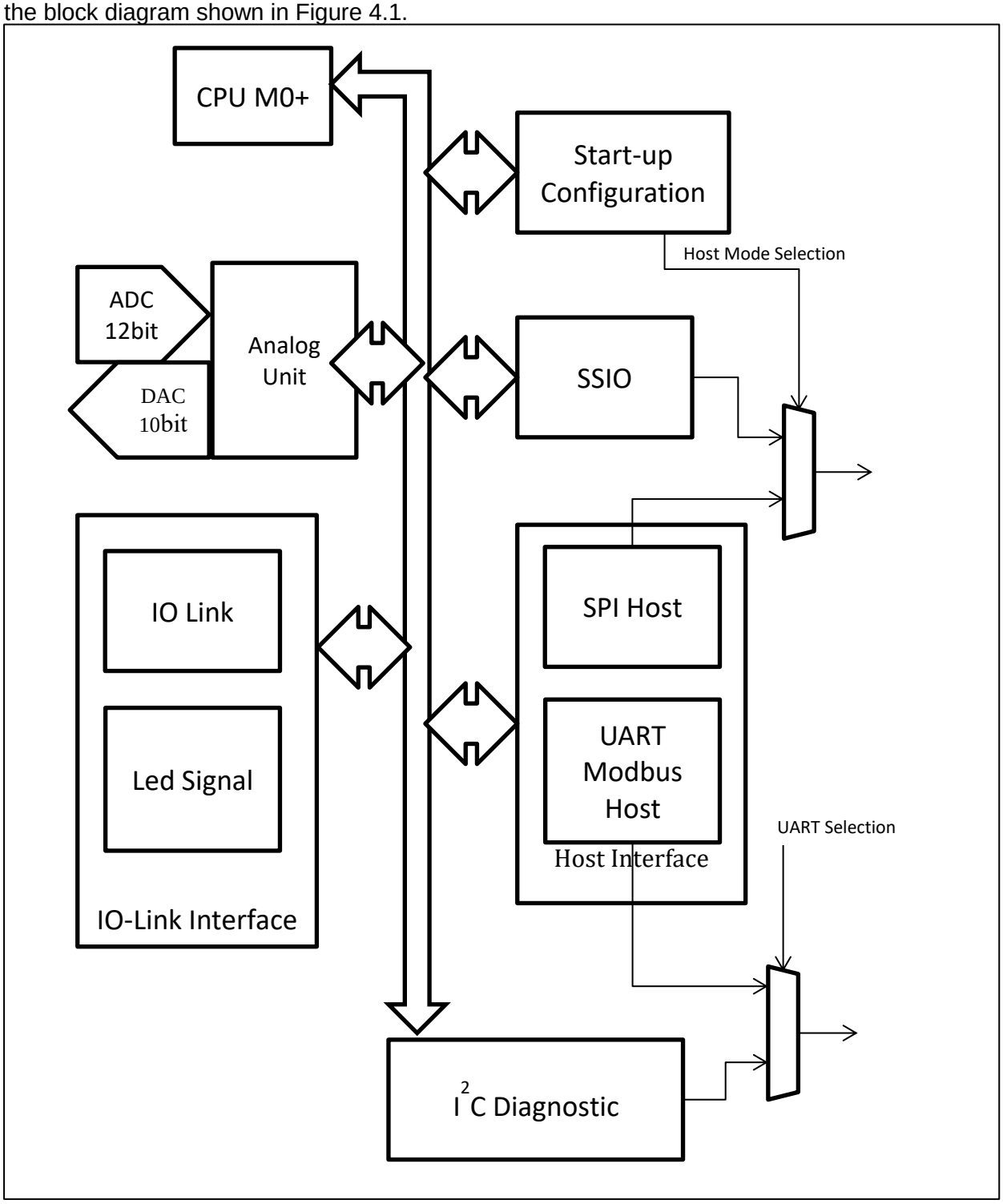


Figure 4.1. Block Diagram

4.2 CPU

The ARM Cortex-M0+ core runs at an operating frequency of 30 MHz and it manage all functionality of IOLS-E module. In simple operation its principal activity is to exchange data process IN and OUT with IO-Link Interface, and cyclically run SSIO (Serial Shifter IO) interface for read and write data from/to field.

4.3 Start-Up Configuration

At start-up the IOLS-E module put CFGx pins into input state with internal pull-down enabled. In function of hardware implementation, the module, in automatic, establishes some configuration for work after start-up. In particular, it will define if module works into SSIO mode or in HOST mode. It will define if in HOST mode is active MODBUS UART interface or only SPI interface.

Refer to the follow table for list of the configurations defined.

Note: For use module into APPLICATION mode you don't need a boot configuration, is another mode to use of the module. For details refer to chapter 4.8: Application mode feature.

Configuration HW Pin				Module Configuration mode	Configuration parameters	Data image Slave to/form Master IO-Link										
Pin CFGSSIO	Pin CFG2	Pin CFG1	Pin CFG0			B00	B01	B02	B03	B04	B..	B07	B..	B11	B..	B31
0	0	0	0	SIMPLE MODE Autonomous functionality with SSIO (Shift register) and ANALOG channel	4byte ANA; 4byte SSIO (8 PDIN, 4 PDOUT)	AN0	AN0	AN1	AN1	SR0	SR..	SR3	X	X	X	X
0	0	0	1		4byte ANA; 8byte SSIO (12 PDIN, 8 PDOUT)	AN0	AN0	AN1	AN1	SR0	SR..	SR3	SR..	SR7	X	X
0	0	1	0		4byte ANA; 28byte SSIO (32 PDIN, 28 PDOUT)	AN0	AN0	AN1	AN1	SR0	SR..	SR3	SR..	SR7	SR..	SR27
0	0	1	1		4byte SSIO (4 PDIN, 4 PDOUT)	SR0	SR1	SR2	SR3	X	X	X	X	X	X	X
0	1	0	0		8byte SSIO (8 PDIN, 8 PDOUT)	SR0	SR1	SR2	SR3	SR4	SR..	SR7	X	X	X	X
0	1	0	1		32byte SSIO (32 PDIN, 32 PDOUT)	SR0	SR1	SR2	SR3	SR4	SR..	SR7	SR..	SR11	SR..	SR31
0	1	1	0		Reserved for use future	Undefined										
0	1	1	1													
1	0	0	0	HOST MODE Need external host. Module communication IO-Link protocol feature only	Use Serial Modbus host interface*	Host depend - Cyclic Data Exchange registers										
1	0	0	1		Use SPI register access host interface	Host depend - Cyclic Data Exchange registers										
1	0	1	0		Reserved for use future	Undefined										
1	0	1	1													
1	1	0	0													
1	1	0	1													
1	1	1	0													
1	1	1	1													

NOTE: 1 = pull-up resistor; 0 = not mount
* Modbus RTU interface is ever enabled.

4.4 Host Interface

Host Interface in the IOLS-E module implements two different ways for connect an external microcontroller. This external microcontroller uses the module for communicate on IO-Link interface, leaving itself free for application activities. In this case module IOLS-E has only communication tasks function.

This is possible using SPI interface or UART Modbus interface.

- SPI interface uses internal SPI peripheral, configured in slave mode. The maximum frequency clock is 5Mbit/s. External host must be configured as master SPI, and must provide clock for communicate with module. Module IOLS-E offers also Slave Select pin functionality to share serial bus with other SPI peripheral into application.

  Follow table see interested pins for SPI interface:

Pin	Name	Description
10	$\overline{SS}$	Select slave input.
11	MISO	Slave Data Output signal.
12	MOSI	Slave Data Input signal.
13	SCLK	Serial clock input signal provided from master on SPI bus.
14	DIRQ	Output signal, Data Interrupt Request. For synchronize host to IO-Link cycle data process exchange.

Table 4.4.1 – Pins for SPI Interface

Data length of SPI communication is 16 bits.
Clock polarity is High, and Data is read on pin MOSI at each rising SCK edge; and Data is made available on pin MISO at each falling SCK edge.

The LSB of the address word is a WR / RD bit, where a '1' indicates that each byte will be written to the registers. Where a ‘0’ indicates that each byte will be reading from the registers.

Valid data is always made available on the MISO line independent of the WR / RD bit. Where a register is written and read in the same operation, then the read value will be the old register value. During read operations, the level of the MOSI line is ignored for the data bytes.

Note: When you write to address Data image, on the MISO line you receive the address data image opposite. View Data Model chapter rules.

Each transmission sequence consists of a falling SS edge which synchronizes transmission, followed by a target register address word. And after data words. Each transmission sequence is close with a rising SS edge.

Note: Attention write correct size otherwise you overwrite other consecutive address registers.
The below figure shows a sequence access with single register or consecutive:

Consecutive access	SS ⌐ MOSI: A D_N D_{N+1} D_{N+2} D_{N+3} ... ⌐ SS MISO: S D_N D_{N+1} D_{N+2} D_{N+3} ...
Single access	SS ⌐ MOSI: A D ⌐ SS MISO: S D
A: Address Word S: Status Word D: Data Word	

Figure 4.4.1 – SPI sequence access

The SPI access must respect follow timing diagram for permit correct access to registers.
Follow image and table show timing:

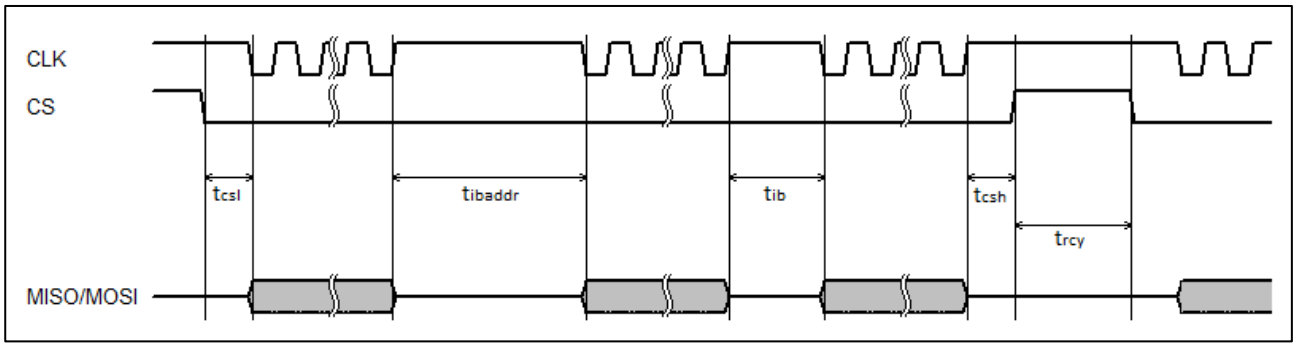


Figure 4.4.2 – Time diagram SPI host mode

	Description	Min	Typ	Max	Unit
Tcsl	Time after chip select active, before start communication	3	5	-	us
Tibaddr	Time inter-byte after first 16bit communication with register address and access request. (Byte word is 16 bits)	24	30	-	us
Tib	Time inter-byte for data communication. (Byte word is 16 bits)	3	5	-	us
Tcsh	Time at end of communication before release chip select and close communication	3	5	-	us
Trcy	Time between two access by SPI communication. Before new active chip select.	4,6	10	-	us

Table 4.4.2 – Time diagram SPI host mode

- UART Modbus interface, work directly on UART asynchronous peripheral, and implemented Modbus Protocol for exchange data and configuration direct on register. The maximum baud rate supported is 512Kbit/s. Modbus is a slave device (Server device) and host CPU must be master Modbus. Module IOLS-E supports the following Modbus function codes:
  - 03 Read Multiple Holding Register
  - 16 Write Multiple Holding Register

  Follow table see interested pins for UART Modbus interface:

n.Pin	Name	Description
21	UART_TX	Asynchronous Serial communication TX module signal.
20	UART_RX	Asynchronous Serial communication RX module signal.
14	DIRQ	Output signal, Data Interrupt Request. For synchronize host to IO-Link cycle data process exchange.

Table 4.4.3 – Pins for UART Modbus Interface

In add feature when configure HOST mode, you can use signal DIRQ for synchronize your application with IO-Link cycle of data process exchange. This function is available both on SPI interface that on UART Modbus Interface.

Host interface works in alternative to Serial Shift IO Interface and Analogical Unit. And must be configured if host is in UART interface.

Host interface works direct on internal area memory dedicated to exchange data with microcontroller. The access to this area is executed from both the SPI interface and the Modbus interface, in according with protocol rules.

In follow chapter is possible to have details on protocol and mapping of area memory:

- Chapter 5.2: Data Model

4.5 Serial Shift IO Interface

The Serial Shift IO Interface permits a simple use of the module IOLS-E without external host. This interface manages external low-cost shift register input and output, allowing you enlarge the amount of available IO digital signal and other.

Peripheral works in alternatives to Host interface. In fact, it works on same pins of SPI host communication. In this case internal peripheral SPI is configured in Master mode, the MISO pin works as SDI line and the MOSI pin as SDO line. The peripheral also adds digital pins to give commands of latching.

Pin	Name	Description
10	LOUT	This signal represents the Latch Output Data, i.e. the data taken over from the shift register into the output register with the rising edge of

		that signal. The signal is also denominated as Load-Out.
14	LIN	This signal represents the Latch Input Data of the serial shift IO interface. The signal is also denominated as Load-In. It works as follows: Signal at low level sets the flip-flops of the shift registers at the level of their parallel input data. Signal at high level saves the input data which then can be read out serially.
11	SDI	This signal represents the Serial Input Data to be received from the serial shift IO interface flip-flops, the MSB is transmitted at first.
12	SDO	This signal represents the Serial Output Data to be transferred into the serial shift IO interface flip-flops. The MSB is transmitted at first.
13	CLK	This signal represents the clock signal for the serial shift IO interface for input and output data. Shifting or latching the data takes place with the leading edge of the SSIO_CLK signal.

Table 4.5 – Pins for Seril Shift IO Interface

The typical cycle of the peripheral, that executes, is:

1. command Load-In latch;
2. data exchange on serial shift IO for input and output. The same clock synchronizes both write and read together (suggest to use same number of shift registers IN and OUT);
3. sends command Load-Out for applied output signal.

If you add Analogical Unit peripheral, you have a complete and flexible stand-alone component able to exchange digital and analog signal of your application directly to IO-Link master board without auxiliary external microcontroller. This solution is very good for simple application that not need particular elaborations of data.

4.6 Analog Unit

When use module IOLS-E in standalone without external microcontroller, there is available also two analog Input channels and one analog output channel, that permit direct connection of the sensor signal and or control analog signal. The module, in this case, takes conversion value and communicates it on IO-Link interface, after minimal digital filtering for noise and takes value from IO-Link interface and sets this on Digital-To-Analog pin.

Is important that analog signal of sensor must have external conditional component dedicated in function of application and signal type. The range scale of ADC internal is defined from AVDD and AGND power supply pins. Maximum value is VDD and DGND (0-3.3V). For best performance, tie AVDD/VREFP and AGND/VREFN at the same voltage levels as VDD and DGND. When selecting VREFP and VREFN different from VDD and DGND, ensure that the voltage midpoints are the same:

(VREFP-VREFN)/2 + VREFN = VDD/2

For a better acquisition and for to maintain a low noise, you can use an analog ground reference dedicate and a inductor filter on AVDD. It depends from your layout and application specification. If there isn't a dedicated power supply for analog unit, remember to close a pin AGND with GND and AVDD with VDD.

The ADC is 12bits resolution successive approximation analog to digital converter. The sampling frequency is up to 100KSample/s for each channel.

The DAC is 10bits resolution resistor string architecture. The sampling frequency is up to 100KSample/s.

Pin	Name	Description
6	AN0	Analog Input signal 0 – Direct to ADC input without conditional signal circuit
7	AN1	Analog Input signal 1 – Direct to ADC input without conditional signal circuit
17	DAC0	Analog Output signal 0 – Direct from DAC output without conditional signal circuit
4	AVDD/ VREFP	Analog supply and positive voltage reference
5	AGND/ VREFN	Analog ground supply and negative voltage reference

Table 4.6 – Analog Input/Output Pins

4.7 IO-Link Interface

The module IOLS-E contains an IO-Link UART peripheral for bidirectional communication on a 3-wire line and stack function, according to the IO-Link Standard specification. In particular according to IO-Link Interface and System Specification Version 1.1.

Peripheral has feature of under-voltage detection, short circuit detection, thermal shutdown protection, and reverse polarization protection.

Furthermore, there is an integrated surge protection for pin IOLINK_GND, IOLINK_CQ and IOLINK_VPLUS to 1kV over 500Ω, half-time 50µs

The interface supports standard baud rate, both 38.4kBaud and 230.4kBaud.

The module IOLS-E can use external LEDs for bus communication status on respective pins. This LEDs are not mandatory in specification document. The developer can choose if add or not them.

Pin	Name	Description
25	IOLINK_GND	Ground IO-Link
24	IOLINK_CQ	IO-Link data signal
23	IOLINK_VPLUS	IO-Link supply voltage
8	LED_BUS1	LED bus status signal Bus OK (Optional in IO-Link specification).
9	LED_BUS2	LED bus status signal Bus Fault (Optional in IO-Link specification)

Table 4.7 – IO-Link interface pins

4.8 Application mode feature

If you want to develop your custom application using the CPU on IO-Link slave module, you can use APPLICATION mode with Mechatronics Labs library stack API access.

The main characteristics:

- Cortex M0+, with main clock up to 30MHz
- Library Stack use 32Kbyte Flash of 64Kbyte
- Library Stack use 8Kbyte RAM of 16Kbyte
- On microcontroller are available various peripherals that you can map on each pin of the module – Thanks switch matrix I/O. (You can use PWM with Dead-Band control, CAPTURE, ADC 12bit more channels, DAC 10 bit 1channel, SPI, UART, I2C….)
- Symbol and layout with added two pins for program and debug application.

This solution mode required discloser agreement. If you are interest at this solution, please contact us.

5 Design- In and application information

The typical connection of application, for host mode or stand-alone, mode:

5.1 General information

Reset and power

Module IOLS-E has a digital power supply pin VDD to 3.3V respect to digital ground DGND pin. Module has internal capacitor of 330nF for power supply sustainment.

In additional, it has also a pin VOUT_3V3 that offers output power supply to 50mA load current. This pin permits to give power at your application components directly from IO-Link Vplus in according with IO-Link specification. This internal regulator has already an internal capacitor, 4.7µF, in order to stable output supply and manage peak current request.

Pin	Name	Description
1	DGND	Device ground supply
2	VOUT_3V3	Output supply, limited to 50mA current load. Offers sensor and application power supply.
3	VDD	Supply voltage for the I/O pad ring, the core voltage regulator, and the analog peripherals.
4	AVDD	Analog supply voltage and positive reference
5	AGND	Analog ground supply and negative reference

Table 5.1 – Reset and Power Pins

You can use a different connection solution, depend from your application. In next figures you can see the different cases.

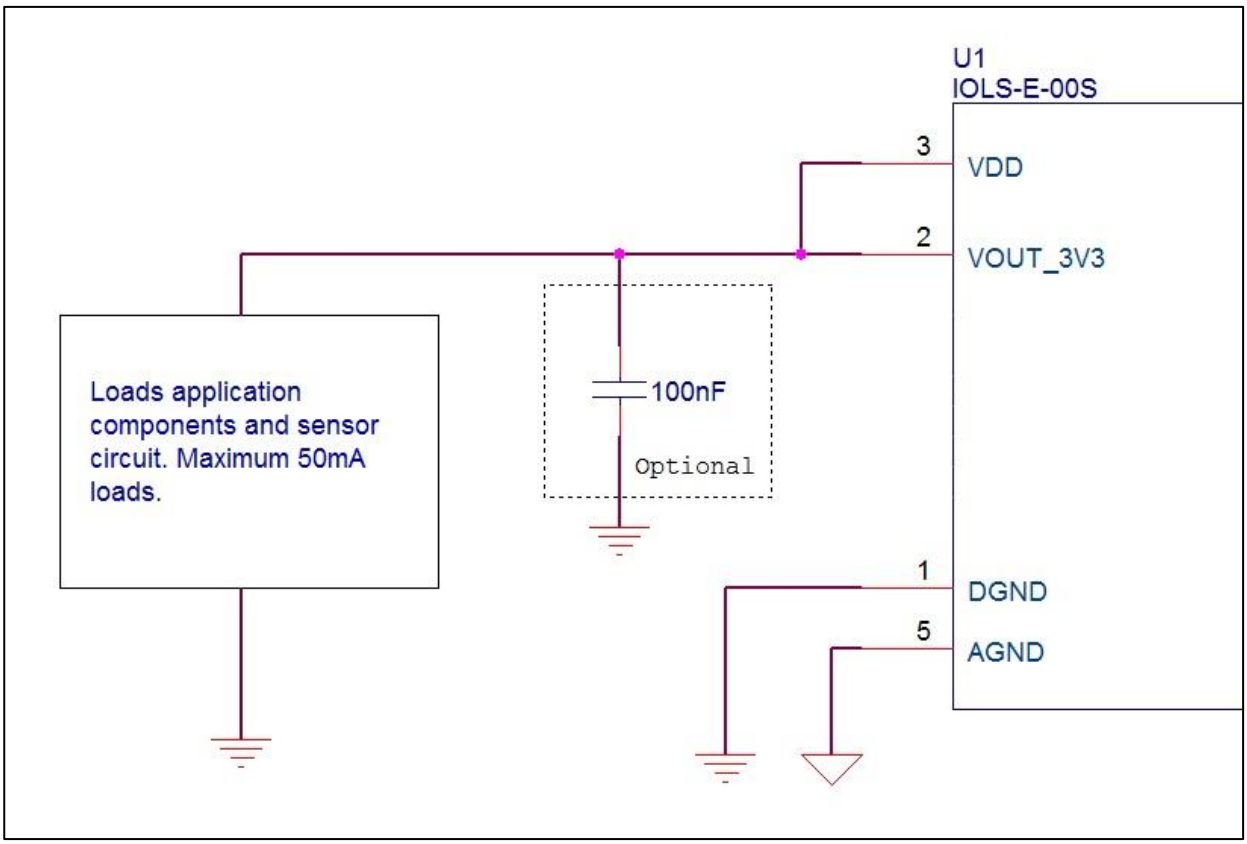


Figure 5.1.1 Power connection directly from IO-Link Type A.

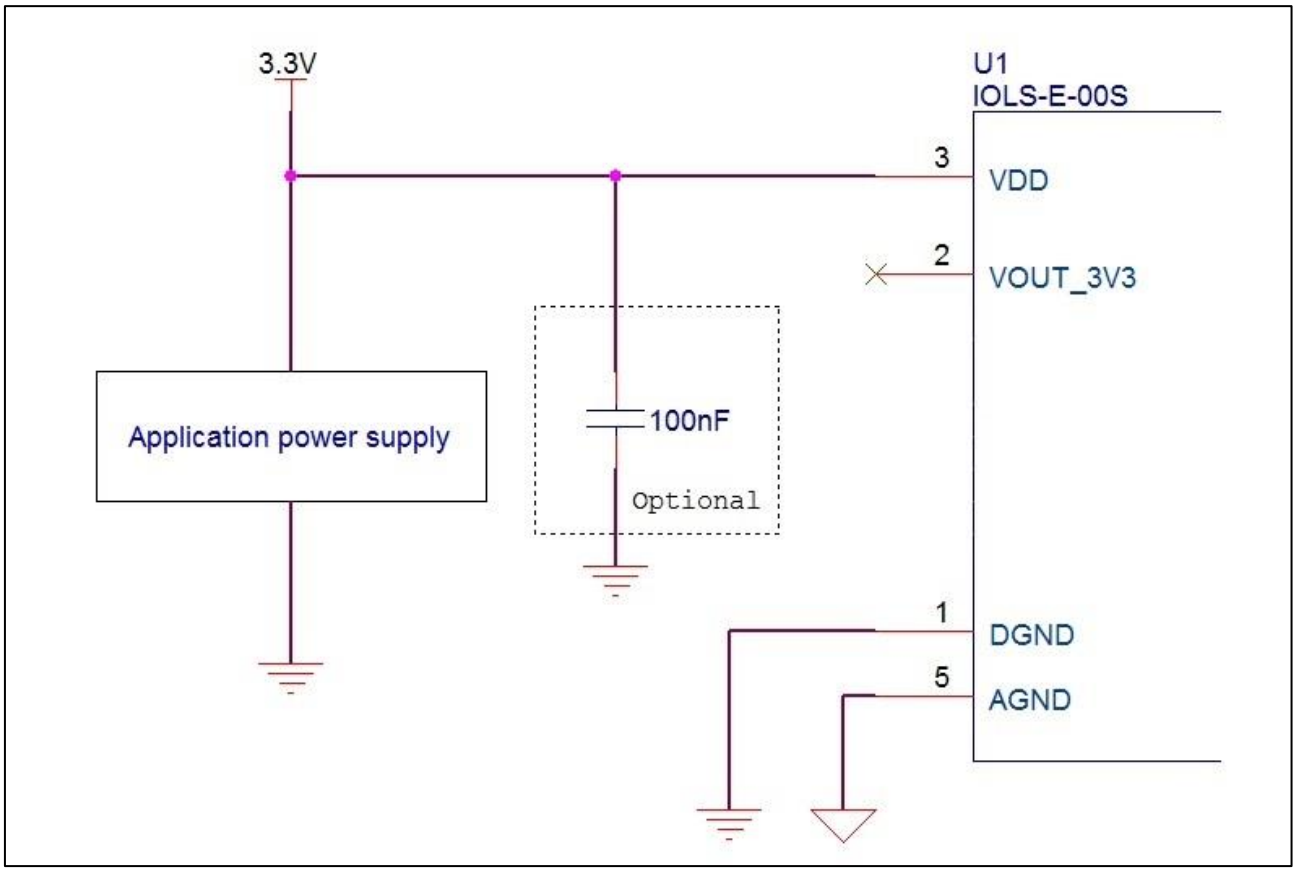


Figure 5.1.2 Power connection from application power supply.

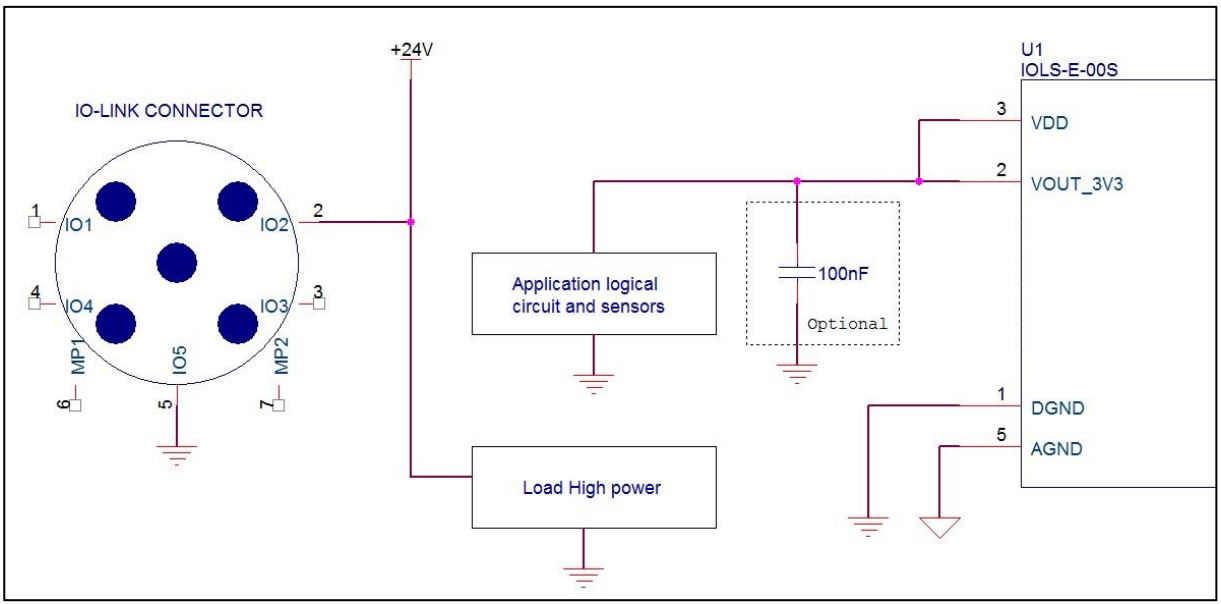


Figure 5.1.3 Power connection directly from IO-Link Type B for loads, and Type A for logic and sensors.

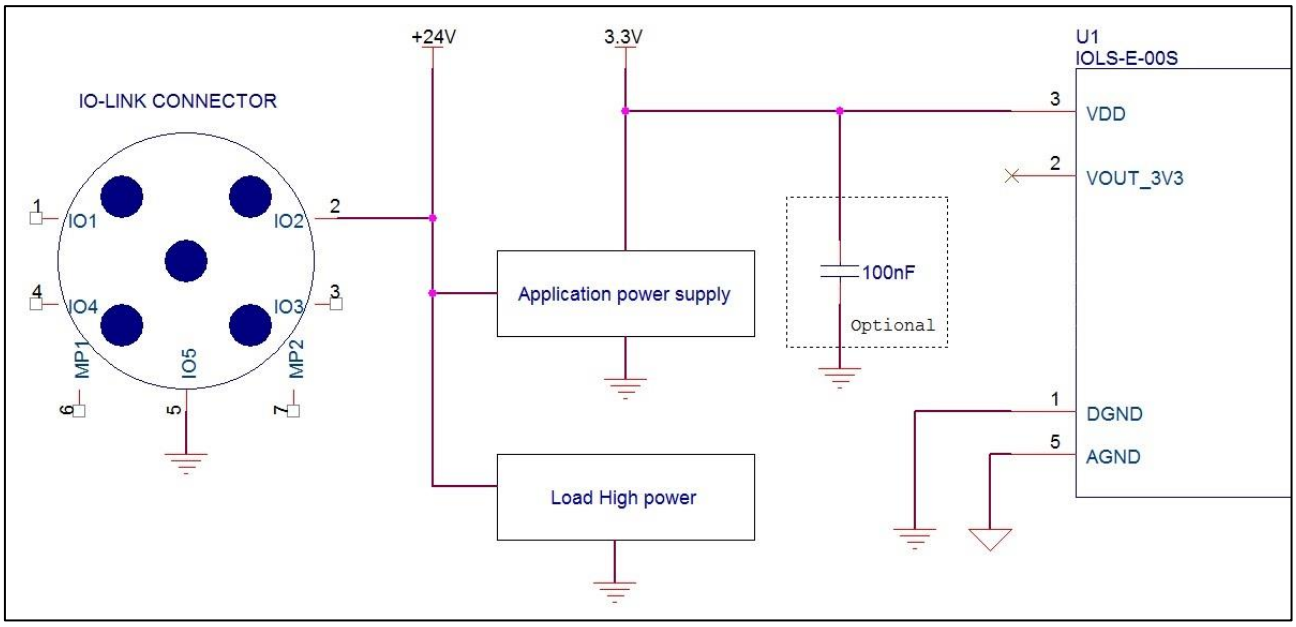


Figure 5.1.4 Power connection directly from IO-Link Type B, but thought power supply application.

External reset input: a LOW-going pulse, as short as 50 ns, on this pin resets the device. This cause that:
- the I/O ports and the peripherals take on their default states, and
- the module restarts the execution of begin to the boot, where the start-up configuration is checked.

The RESET pin not needs external pull-up because has internal pull-up. The RESET can be left unconnected if an external RESET function is not needed.

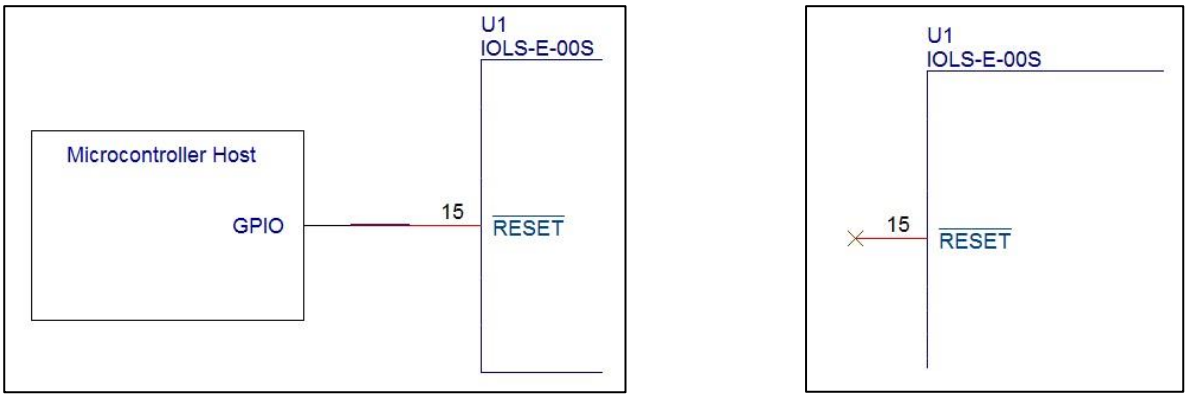


Figure 5.1.5 External Reset command or unconnected.

IO-Link connection and bus LEDs

IO-Link ground is the same ground of the system. Internal of the module IOLS-E has already passive component for correct work. Is suggested, in layout design, to put module near to the connector, and to use internal module ground for link ground together. This in order to not have any issue versus surge and electromagnetic test.

Module IOLS-E Internal schematic view for IO-Link interface:

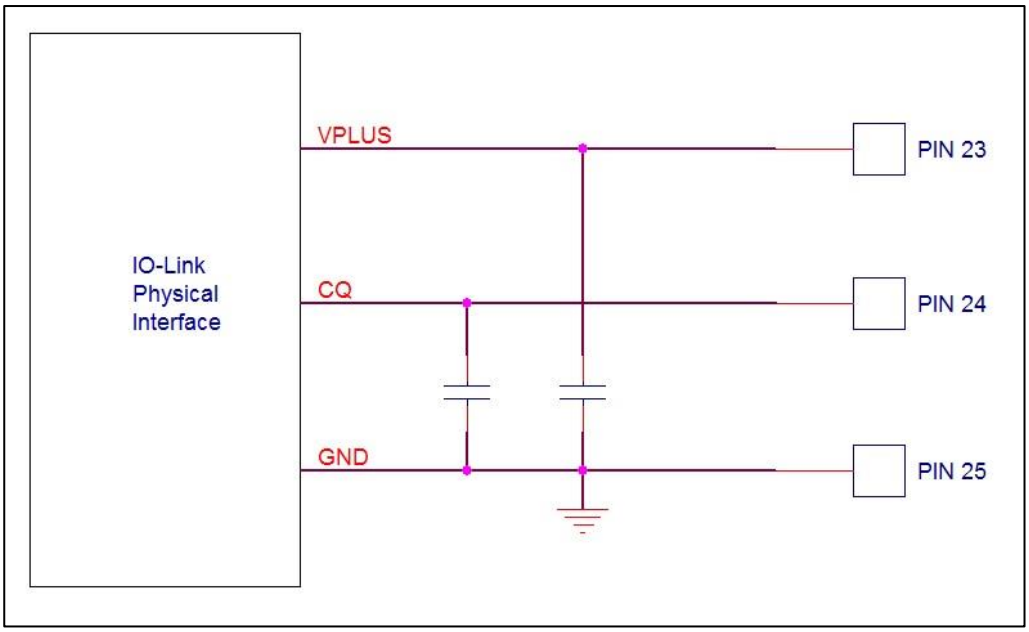


Figure 5.1.2 Internal schematic view for IO-Link interface

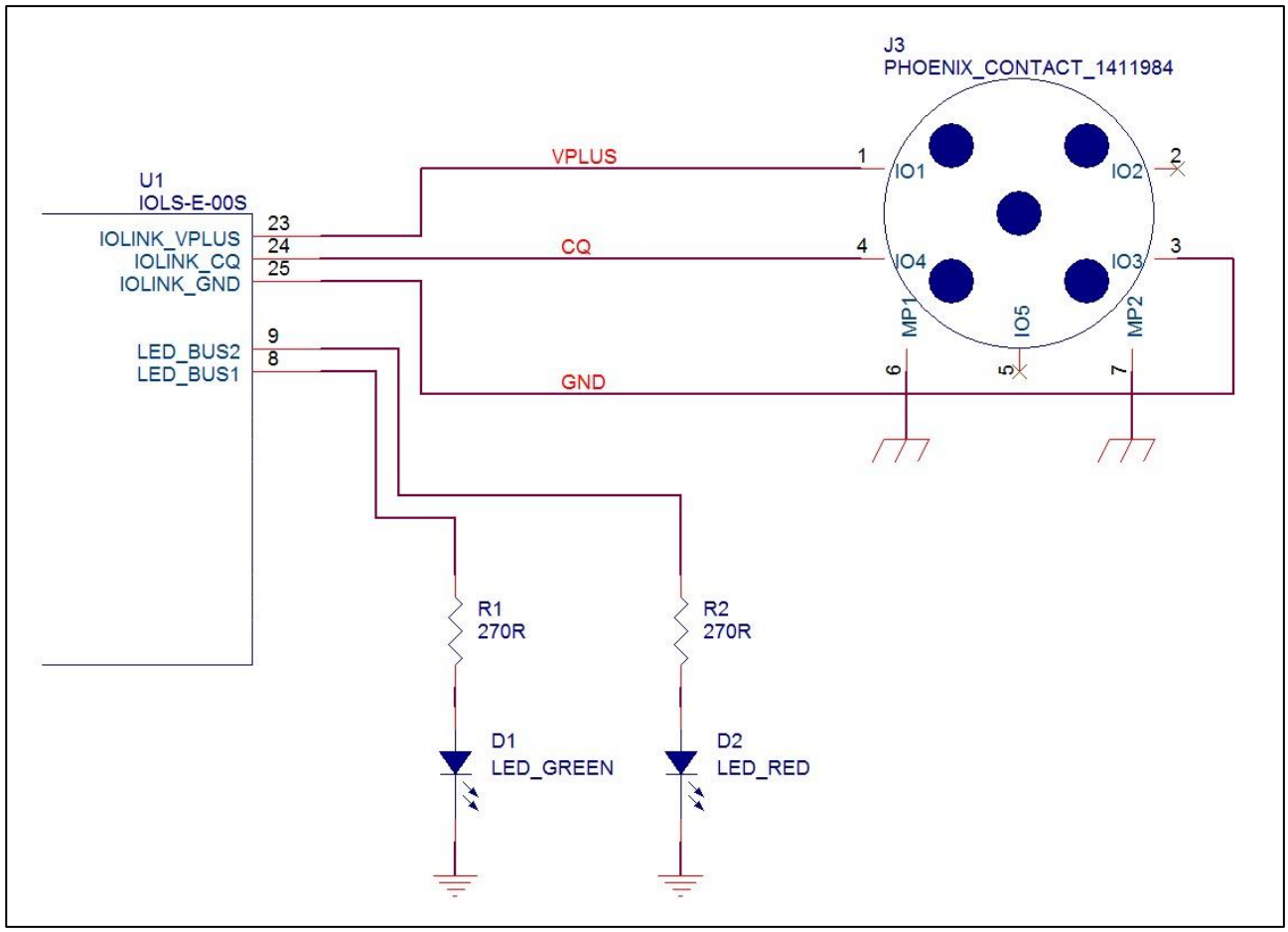


Figure 5.1.3 Typical IO-Link interface connection Type A.

SSIO

The following figure shows to you, how develop your I/O expansion with Serial Shift Input and Output functional.

The SSIO cycle permits to use different number of Shift register between INPUT and OUTPUT. But cycle and IO-Link communication work with maximum configuration choice in start-up.

For Example: You set start-up configuration for 4 bytes IN and 4 bytes OUT but you put 2 shifts register for input and 1 shift register for output. In this case cycle on SSIO and IO-Link exchange data work for 4 bytes IN and OUT.

Note: If you using Analog Unit, you must consider that 4 bytes of INPUT data process are busy, therefore you have maximum 28 byte for Digital Input, 28 shift register. But you can use 32 bytes for Digital Output. If you not use Analog Unit 32 bytes + 32 bytes are permit.

Note: The logic order of input and output in figure, is same order that you have in master PLC, in particular:

Data INPUT memory image with Analog Unit:

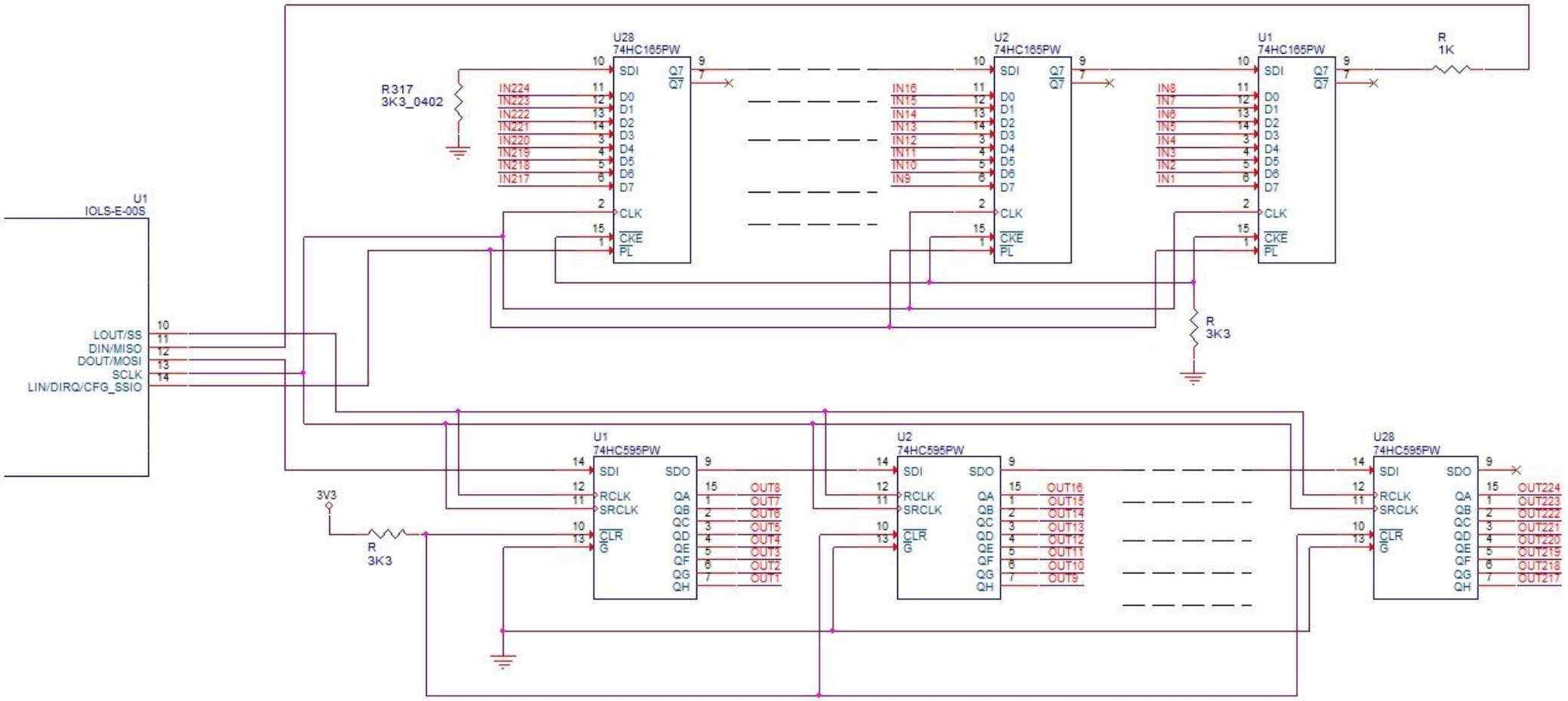
Offset in data memory image	**MSB Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**LSB Bit0**
Offset 0							High Byte AN0	
Offset 1	Low Byte 12bit conversion AN0							
Offset 2							High Byte AN1	
Offset 3	Low Byte 12bit conversion AN1							
Offset 4	IN8	IN7	IN6	IN5	IN4	IN3	IN2	IN1
Offset 5	IN16	IN15	IN14	IN13	IN12	IN11	IN10	IN9
….								
Offset 31	IN224	IN223	IN222	IN221	IN220	IN219	IN218	IN217

Data INPUT memory image without Analog Unit:

Offset in data memory image	**MSB Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**LSB Bit0**
Offset 0	IN8	IN7	IN6	IN5	IN4	IN3	IN2	IN1
Offset 1	IN16	IN15	IN14	IN13	IN12	IN11	IN10	IN9
….								
Offset 31	IN256	IN255	IN254	IN253	IN252	IN251	IN250	IN249

Data OUTPUT memory image without Analog Unit:

Offset in data memory image	**MSB Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**LSB Bit0**
Offset 0	OUT 8	OUT 7	OUT 6	OUT 5	OUT 4	OUT 3	OUT 2	OUT 1
Offset 1	OUT 16	OUT 15	OUT 14	OUT 13	OUT 12	OUT 11	OUT 10	OUT 9
….								
Offset 31	OUT 256	OUT 255	OUT 254	OUT 253	OUT 252	OUT 251	OUT 250	OUT 249

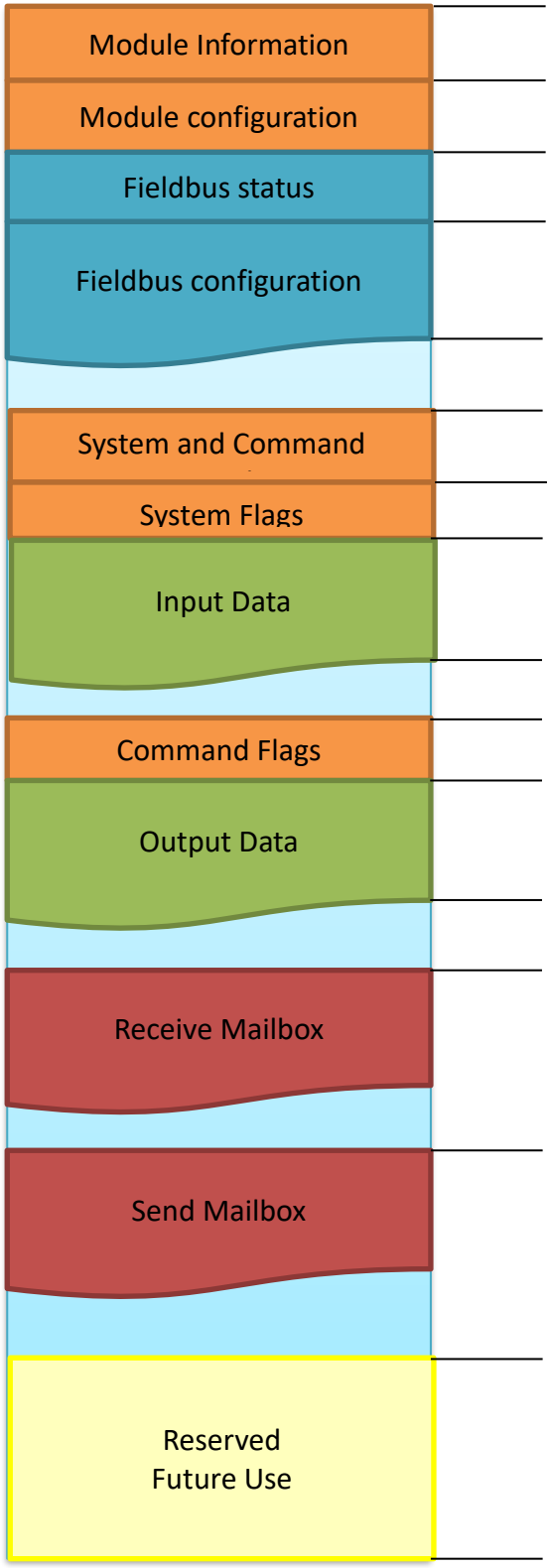

U1
IOLS-E-00S
LOUT/SS
DIN/MISO
DOUT/MOSI
SCLK
LIN/DIRQ/CFG_SSIO
3V3
R
3K3
R317
3K3_0402
U28
74HC165PW
U2
74HC165PW
U1
74HC165PW
R
1K
R
3K3
SDI
Q7
D0
D1
D2
D3
D4
D5
D6
D7
CLK
CKE
PL
IN224
IN223
IN222
IN221
IN220
IN219
IN218
IN217
IN16
IN15
IN14
IN13
IN12
IN11
IN10
IN9
IN8
IN7
IN6
IN5
IN4
IN3
IN2
IN1
U1
74HC595PW
U2
74HC595PW
U28
74HC595PW
SDI
SDO
RCLK
SRCLK
CLR
G
QA
QB
QC
QD
QE
QF
QG
QH
OUT8
OUT7
OUT6
OUT5
OUT4
OUT3
OUT2
OUT1
OUT16
OUT15
OUT14
OUT13
OUT12
OUT11
OUT10
OUT9
OUT224
OUT223
OUT222
OUT221
OUT220
OUT219
OUT218
OUT217

5.2 Data Model

The Register Area of the serial Host Interface at the virtual Dual-Port-Memory is the central point connecting all interfaces. This Register Area has a fixed structure and is divided in different Data Areas for the

- IO-Link Fieldbus-System,
- the shift registers and analog unit,
- and internal Information, Configuration and Status structures.

The Host-System can read and, if write access is allowed, also write at all addresses with different amount of data by using Modbus RTU functions or SPI register access.
If the host wants to exchange data over Fieldbus, the host has to write the data at the corresponding place of the Output Data Area respectively the host has to read it out of the Input Data Area.
When the module IOLS-E works as a Modbus RTU Slave, the Modbus RTU Master can read with function code 3 from the register area and write with function code 16 into the register area of the module IOLS-E.


Module Information
Module configuration
Fieldbus status
Fieldbus configuration
System and Command
System Flags
Input Data
Command Flags
Output Data
Receive Mailbox
Send Mailbox
Reserved
Future Use

Register Address	Data Type and Size	Description	Access
0…49	UINT8[100]	Module Information	RO
50…99	UINT8[100]	Module configuration	RW
100…149	UINT8[100]	Fieldbus IO-Link status	RO
150…249	UINT8[200]	Fieldbus IO-Link configuration	RW
250…260	UINT8[22]	Reserved for future use.	
261…262	UINT32	System Status	RO
263…266	UINT32[2]	Reserved for future use.	
267…268	UINT32	System Error	RO
269…284	UINT32[8]	Error History and Log. Not available now. Future improvement.	RO
285	UINT16	Error counter	RO
286…289	UINT32[2]	Reserved for future use.	
290…291	UINT32	Communication Error	RO
292…293	UINT32	Communication Status	RO
294…297	UINT32[2]	Reserved for future use.	
298…299	UINT32	System Flags	RO
300…349	UINT8[100]	Process Data Input image; IO-Link Device to Master (Cyclic Data Exchange)	R/W
350…397	UINT8[96]	Reserved for future use.	
398…399	UINT32	Command Flags	R/W
400…449	UINT8[100]	Process Data Output image; IO-Link Master to Device (Cyclic Data Exchange)	RO
450…499	UINT8[100]	Reserved for future use.	
500…573	UINT8[148]	Receive mailbox Packet (Acyclic Data)	RO
574…599	UINT8[52]	Reserved for future use.	
600…673	UINT8[148]	Sent mailbox Packet (Acyclic Data)	RW

674…699	UINT8[52]	Reserved for future use.	
700…799	UINT8[200]	User Data Not available now. Future improvement.	RW

Table 5.4.1 – Register area

The following rules are applied:

- Unused areas are initialized with 0.
- You can access each of these registers externally from host using a Master via the serial Modbus RTU protocol or via SPI register access.
- PDIN is defined Process Data Input (viewed from IO-Link Master side)
- PDOUT is defined Process Data Output (viewed from IO-Link Master side)
- In SPI communication, for cyclic access performance, when you write address 300 module responses with address 400. In this way with unique access you can write PDIN and read PDOUT data. This is possible only with SPI communication interface.

Module Information Block

The Module Information Block consists of the following elements:

Start Register	Data Type and Size	Description
0	UINT16	Device Type
1	UINT8	Hardware revision
1	UINT8	Hardware compatibility index (unused, initialized with 0)
2	UINT32	Hardware Options
4	UINT8[8]	Reserved
8	UINT8[8]	Firmware version of the loaded firmware
12	UINT8[4]	Firmware Date of the loaded firmware
14	UINT8[16]	Firmware Name of the loaded firmware
22	UINT8[8]	Reserved
26	UINT16	Communication Class of the loaded firmware (unused, initialized with 0)
27	UINT16	Protocol Class of the loaded firmware (unused, initialized with 0)
28	UINT16	Protocol Conformance Class of the loaded firmware (unused, initialized with 0)

29	UINT32	Virtual Dual Port Memory Size
31…49	UINT8[38]	Reserved

Device Type (Register 0)

This field identifies the hardware.

The following hardware device type have been defined for the IOLS-E module, depending on the functionality of module:

IOLS-E function	Device ID
Sensors	0x0001

Hardware revision and compatibility index (Register 1)

Low Byte:

Hardware revision:

This field indicates the current hardware revision of a module. It starts with 1 and is incremented by 1 with every significant hardware change.

High Byte:

Compatibility index (not used, is initialized with 0):

The hardware compatibility index starts with zero and is incremented every time changes to the hardware require incompatible changes to the firmware.

Hardware Options (Register 2)

Future implementation.

Firmware version of the loaded firmware (Register 8)

The firmware version of the currently loaded firmware.

Byte 0 Decimal revision mayor change
Byte 1 Decimal revision minor change
Byte 2 Low byte decimal revision internal information
Byte 3 High byte decimal revision internal information
Byte 4 Reserved
Byte 5 Reserved
Byte 6 Reserved
Byte 7 Reserved

Firmware Date of the loaded firmware (Register 12)

The firmware date of the currently loaded firmware

Byte 0 Low byte decimal date Year
Byte 1 High byte decimal date Year
Byte 2 Decimal date Month
Byte 3 Decimal date Day

Example:

Date = 2017-02-15
Byte 0 = 0xE1
Byte 1 = 0x07
Byte 2 = 0x02
Byte 3 = 0x0F

Firmware Name of the loaded firmware (Register 14)

The firmware name of the currently loaded firmware.

Note: The first byte in the firmware name represents the length of the firmware name, then the characters follow.

Virtual Dual Port Memory Size (Register 29)

Virtual Dual Port Memory Size (IOLxE_RegArea.h) expressed in bytes.

The Virtual Dual Port Memory can be accessed both from the IOLink module and from the master.

Module Configuration Block

The Module Configuration Block consists of the following elements:

Start Register	Data Type and Size	Description
50	UINT16	HW Startup configuration setup
51	UNIT16	Simple/host mode
52	UNIT16	ADC interface enabled/disabled
53	UNIT16	Endian mode of ADC values SSIO data
54	UNIT16	ADC index/offset byte
55	UNIT16	SSIO interface enabled/disabled
56	UNIT16	SSIO address Default set to 0
57	UNIT16	Endian mode of SSIO data: big endian/little endian
58	UNIT16	Shift order starting of SSIO Process Data
59	UNIT16	Maximum number of SSIO Process Data In and/or Out
60	UNIT16	Number of Process Data elements output from SSIO
61	UNIT16	Number of Process Data elements input from SSIO
62	UNIT16	HOST interface
63	UNIT16	Endian mode of HOST data: big endian/little endian
64	UNIT16	Number of Process Data elements output from HOST
65	UNIT16	Number of Process Data elements input from HOST
66	UNIT16	Reserved
67	UNIT16	MDB interface
68	UNIT16	Modbus slave identification number
69	UNIT16	Modbus UART Speed
70	UNIT16	Modbus UART Data length
71	UNIT16	Modbus UART Stop bit
72	UNIT16	Modbus Parity type

73	UNIT16	Endian swap of Tx/Rx params from/to device memory
74	UNIT16	Reserved
75	UNIT16	Number of Process Data elements output from MDB
76	UNIT16	Number of Process Data elements input from MDB
77…87	UNIT16[11]	Critical values. Not accessible
88…99	UNIT16[12]	Reserved

HW Startup configuration setup (Register 50)

Loads the external configuration input

0 = Disable
1 = Enable (Default)

Simple/host mode (Register 51)

0 = Simple (Default)
1 = Host mode

ADC interface (Register 52)

Enable the Analog Digital Converter module

0 = Disable
1 = Enable (Default)

Endian mode of ADC values SSIO data (Register 53)

1 = Big endian
2 = Little endian (Default)

ADC index/offset byte (Register 54)

Offset of cyclical data. Default = 0

SSIO interface (Register 55)

Enable the Simple Serial IO module

0 = Disable
1 = Enable (Default)

SSIO address (Register 56)

SSIO address of the connected device. Default = 0

Endian mode of SSIO data (Register 57)

1 = Big endian
2 = Little endian (Default)

Shift order starting of SSIO Process Data (Register 58)

1 = idx low, bottom to top
2 = idx hig, top to bottom (Default)

Maximum number of SSIO Process Data In and/or Out (Register 59)

Default: 8

Number of Process Data elements output from SSIO (Register 60)

Default: 7

Number of Process Data elements input from SSIO (Register 61)

Default: 4

HOST interface (Register 62)

Enable the HOST module

0 = Disable
1 = Enable (Default)

Endian mode of HOST data (Register 63)

1 = Big endian
2 = Little endian (Default)

Number of Process Data elements output from HOST (Register 64)

Default: 32

Number of Process Data elements input from HOST (Register 65)

Default: 32

MDB interface (Register 67)

Enable the Modbus module

0 = Disable
1 = Enable (Default)

Modbus slave identification number (Register 68)

Default = 2

Modbus UART Speed (Register 69)

Default = 9600

Modbus UART Data length (Register 70)

Default = 8

Modbus UART StopBit (Register 71)

Default = 1

Modbus Parity type (Register 72)

UART Parity type:

0 = None (Default)
1 = Even
2 = Odd

Endian swap of Tx/Rx params from/to device memory (Register 73)

Swap between the most significative byte and the less significative one.

1 = Big endian
2 = Little endian (Default)

Number of Process Data elements output from MDB (Register 75)

Default: 32

Number of Process Data elements input from MDB (Register 76)

Default: 32

Fieldbus IO-Link Status Block

The Fieldbus IO-Link Status Block manages the Fieldbus IO-Link connection reports and consists of the following elements:

Start Register	Data Type and Size	Description
100	UINT16	IO-Link Fieldbus connected/disconnected
101	UINT16	IO-Link Fieldbus protocol state
102	UINT16	IO-Link Fieldbus protocol standard error code
103	UINT16	IO-Link Fieldbus error count since last power-on
104	UINT16	IO-Link Watchdog timeout set
105…149	UINT8[90]	Reserved

IO-Link Fieldbus connected/disconnected (Register 100) bus_changeOfState

Not available now. Future improvement.

IO-Link Fieldbus protocol state (Register 101) bus_state

Not available now. Future improvement.

IO-Link Fieldbus protocol standard error code (Register 102) bus_err

Not available now. Future improvement.

IO-Link Fieldbus error count since last power-on (Register 103) bus_err_count

Not available now. Future improvement.

IO-Link Watchdog timeout set (Register 104) bus_wdog

Not available now. Future improvement.

Fieldbus IO-Link Configuration Block

The Fieldbus IO-Link Configuration Block consists of the following elements:

Start Register	Data Type and Size	Description
150	UINT16	SIO Drive mode
151	UINT16	M-Sequence capability
152	UINT16	Process data input
153	UINT16	Process data output
154	UINT16	IO-Link Protocol revision ID
155	UINT32	IO-Link Device ID
157	UINT32	IO-Link Vendor ID
159	UINT16	Baud rate of IOLink SCI connection
160	UINT16	Minimum IOLink period for cyclic data exchange
161	UINT16	Auto-start flag
162…260	UINT8[198]	Reserved

SIO Drive Mode (Register 150) SIO_driveMode

Simple Input Output Drive mode, has two functions: push up and pull down.

Predefined drive mode is push-pull.

Default: DRIVE_MODE_PUSH_PULL

M-Sequence capability (Register 151) MSEQ_capability

At present only handled by Type_2_v with 1 byte on demand

Future improvement will handle another configuration.

Default: MSEQCAP_ISDU_NOT_SUPPORTED | MSEQCAP_OP_CODE_4 | MSEQCAP_PREOP_CODE_0

Process data input (Register 152) PDin_size

Process data input related to master: IOLSE input

Can vary from 0 to 32 byte.

Default: 32

Process data output (Register 153) PDout_size

Process data output related to master: IOLSE output

Can vary from 0 to 32 byte.

Default: 32

IO-Link Protocol revision ID (Register 154) Revision_id

Currently Revision 1.1

Default: REVISION_ID_1_1

IO-Link Device ID (Register 155) Device_id

Device ID of Mechatronics Labs

Default: 0x10001

IO-Link Vendor ID (Register 157) Vendor_id

Vendor ID of Mechatronics Labs

Default: 0x03E7

Baud rate of IO-Link SCI connection (Register 159) Baud_rate

Choosing from 3 possible Baud rate:

COM1_4800_BAUDRATE

COM2_38400_BAUDRATE (Default, forced)

COM3_230400_BAUDRATE

Minimum IO-Link period for cyclic data exchange (Register 160) Min_cyle_time

Minimum IO-Link period for cyclic data exchange in decims of mSec, predefine is 24 millisec.

Default: 240

Auto-start flag (Register 161)

Define if bus communication goes run automatically or wait external command.

1: Automatic start bus
0: Manual start bus – wait command

Default: 1 into Simple mode configuration, 0 into Host mode configuration

System Status

Start Register	Data Type and Size	Description
261	UINT32	System status
263…266	UINT32[2]	Reserved

System Status (Register 261)

Not available now. Future improvement.

System Error

Start Register	Data Type and Size	Description
267	UINT32	System Error
269...284	UINT32[8]	Error History and Log

System Error (Register 267)

The 32bit address is divided in a 16bit low word and in a 16bit high word due to a bus regard. The error codes use a bit mask to divide the various error types.

Lower 16bit word:

Mask	Description
0x0000000F	Flash Errors
0x000000F0	EEprom Errors
0x00000F00	Physical Fieldbus dev Errors
0x0000F000	Ram Errors

Flash Errors

1. Not found
2. Type error
3. Size error
4. Test fail
5. Access error

EEprom Errors

1. Type error
2. Size error
3. Lock error
4. Initialization error
5. Test fail
6. Not found

Physical Fieldbus dev Errors

1. Type error
2. Initialization error
3. IO error
4. Test fail

Ram Errors

1. Not found
2. Type error
3. Initialization error
4. IO error
5. Test fail
6. Malloc error

Higher 16bit word:

Mask	Description
0x0000000F	Process/Task Errors
0x000000F0	Configuration Errors
0x00000F00	Protocol stack Errors

Process/Task Errors

1. Initialization error

Configuration Errors

1. Setval error
2. Access error

Protocol stack Errors

1. Initialization error
2. Procedural error

Error History and Log (Register 269)

Not available now. Future improvement.

Error Counter

Start Register	Data Type and Size	Description
285	UINT16	Error Counter
286…289	UINT32[2]	Reserved

Error Counter (Register 285)

Not available now. Future improvement.

Fieldbus Communication

Start Register	Data Type and Size	Description
290	UINT32	Communication Error
292	UINT32	Communication Status
294…297	UINT32[2]	Reserved

Communication Error (Register 290)

Not available now. Future improvement.

Communication Status (Register 292)

Not available now. Future improvement.

Flags and Data Block

The Flags and Data Block consists of the following elements:

Start Register	Data Type and Size	Description
298	UINT32	System Flags
300...349	UINT8[100]	Process Data Input image; IO-Link Device to Master (Cyclic Data Exchange)
350...397	UINT8[96]	Reserved
398	UINT32	Command Flags
400...449	UINT8[100]	Process Data Output image; IO-Link Master to Device (Cyclic Data Exchange)
450...499	UINT8[100]	Reserved

System Flags (Register 298)

The 32bit address is divided in a 16bit low word and in a 16bit high word due to a bus regard. The error codes use a boolean bit shift mask to identify the various errors.

Lower 16bit word:

Bit Shift Mask	Description
0	Ready Flag
1	Module error Flag
2	Communication error Flag
3	Network Flag
4	Received mailbox Flag
5	Sent mailbox Flag
6	Bus on Flag
7	Configuration done from flash
8	Configuration locked
9	Configuration watch dog enabled

10	Configuration system running

0. Ready Flag
   If set, running normal operating mode, self-test terminated

1. Module error Flag
   Module error condition, also based on sys_error non-zero value

2. Communication error Flag
   Communication link condition

3. Network Flag
   Fieldbus (IO-Link) protocol error

4. Received mailbox Flag
   Received mailbox busy/not available

5. Sent mailbox Flag
   Received mailbox busy/not available

6. Bus on Flag
   The protocol is active on IO-Link fieldbus

7. Configuration done from flash

8. Configuration locked
   Configuration locked, not writable

9. Configuration watch dog enabled

10. Configuration system running

Higher 16bit word:

Not available now. Future improvement.

Process Data Input image (Register 300)

Default data size is UINT8[100].

Contains Cyclic Process Data sent to IO-Link master. Actual IO-Link standard communication uses 32 bytes.

Command Flags (Register 398)

The 32bit address is divided in a 16bit low word and in a 16bit high word due to a bus regard. The error codes use a boolean bit shift mask to identify the various errors.

Lower 16bit word:

Bit Shift Mask	Description
0	Reserved, Boot request
1	Reserved, Boot ack
2	Reset command flag
3	Bus on
4	Re-Initialization
5	Bus off
6	Clear configuration
7	Store configuration
8	Lock configuration
9	Unlock configuration
10	Enable the system watchdog
11	Disable the system watchdog
12, 13	Reserved, Device and application
14, 15	Application command code

0. Reserved, Boot request
   The host requests a system boot/re-flash

1. Reserved, Boot ack
   The system allows the boot process

2. Reset command flag
   Do a system reset

3. Bus on
   The module will open the available network connection

4. Re-Initialization
   The module and the stack processes will be re-init: needed for configuration changes

5. Bus off
   The module will close the opened network connection, or inhibit to open it

6. Clear configuration
   The stored configuration, if present, will be cleared

7. Store configuration
   The working configuration will be stored in EEprom

8. Lock configuration
   The users will be disabled to perform configuration changes

9. Unlock configuration
   The users will be enabled to perform configuration changes

10. Enable the system watchdog

11. Disable the system watchdog

12. 13. Reserved
    Device and application reserved

14. 15. Application-Specific (fieldbus, host or device application) command code. If non-zero, the full command flag will be used to embed

Process Data Output image (Register 400)

Default data size is UINT8[100].

Contains Cyclic Process Data received from IO-Link master. Actual IO-Link standard communication uses 32 bytes

Mailbox Packet Block

The Mailbox Packet Block consists of the following elements:

Start Register	Data Type and Size	Description
500...599	**UINT8[200]**	**Receive mailbox Packet (Acyclic Data)**
500...508	UINT16[9]	Mailbox header
509...572	UINT8[128]	Received mailbox data
573	UINT16	Last mailbox data by the sender
574…599	UINT8[52]	Reserved
600…699	**UINT8[200]**	**Sent mailbox Packet (Acyclic Data)**
600...608	UINT16[9]	Mailbox header
609...672	UINT8[128]	Sent mailbox data
673	UINT16	Last mailbox data by the receiver
674...699	UINT8[52]	Reserved

Mailbox Header Sub-Block

The Mailbox Header of received and sent mail consists of the following elements:

Start Register	Data Type and Size	Description
500 / 600	UINT16	Source media (phys.chan/dev)
501 / 601	UINT16	Source application layer
502 / 602	UINT16	Destination media (phys.chan/dev)
503 / 603	UINT16	Destination application layer
504 / 604	UINT16	Message command type/code
505 / 605	UINT16	Message error code
506 / 606	UINT16	Message identifier or sequence/part number
507 / 607	UINT16	Total message frame sequence/part
508 / 608	UINT16	Length of the message

Source media (Register 500/600)

ID of the sending device.

Source application layer (Register 501/601)

Application that sent the mail.

Destination media (phys.chan/dev) (Register 502/602)

ID of the receiving device.

Destination application layer (Register 503/603)

Receiving application.

Message command type/code (Register 504/604)

The type or code of the massage.

Not managed yet.

Message error code (Register 505/605)

Not available now. Future improvement.

Message identifier or sequence/part number (Register 506/606)

The ID of the message or his part number of the frame.

Total message frame sequence/part number (Register 507/607)

The total length of the frame.

Length of the message (Register 508/608)

Length of the message in byte, from the first data byte

User Data Block

The User Data Block consists of the following elements:

Start Register	Data Type and Size	Description
700…799	UINT8[200]	User Data

Not available now. Future improvement.

5.3 I²C Bus - Diagnostic protocol

Not available now. Future improvement.

6 COMPONENTS CHARACTERISTICS AND RATINGS

T_{amb} = -40°C to 105°C, unless otherwise specified.

All values refer to GND unless otherwise specified.

6.1 Absolute maximum ratings of module

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.5	+4.6	V
Input voltage	V_I	-0.5	+5.5	V
Analog input voltage	V_{IA}	-0.5	+3.6	V
Supply current	I_{DD}	-	100	mA
I/O Latch-up current	I_{latch}	-	100	mA
Maximum junction temperature	$T_{j(max)}$	-	150	C°
Total power dissipation	P_{tot}	-	0.5	W
Electrostatic discharge voltage	V_{esd}	-	3.5	kV
Storage temperature range		-25	+100	C°
Soldering temp. (20-40sec, cf. JEDEC J-STD-020C)			+260	C°

6.2 IO-Link Group (pin n. 2,23,24,25)

6.1.1 Absolute maximum ratings

Parameter	Min	Max	Unit
Pin voltage IOLINK_VPLUS	-40	+40	V
Pin voltage IOLINK_CQ	-40	+40	V
Pin voltage VOUT_3V3	-1	+7	V

Table 6.1.1 Absolute Maximum Ratings IO-Link

6.1.2 Operating parameters

Description	Symbol	Min.	Typ	Max	Unit	Condition
VPLUS supply voltage, VSNS=3.3V, ISNS=50mA	V_{SUP}	5	24	30	V	
Blocking capacitor on VPLUS	C_{BLK}	100			nF	
EMC blocking capacitor	C_{EMC}		470		pF	
Maximum load capacitor	C_{LOAD_MAX}			250	nF	
Maximum inductance	I_{LOAD_MAX}			††	mH	
VOUT_3V3 supply blocking capacitor	C_{SNS}	1		10	µF	
†† unlimited						

Table 6.1.2 Operating parameters IO-Link

6.1.3 Electrical parameters

Electrical parameters are valid over the operating temperature and voltage range, unless otherwise stated.

Description	Condition	Symbol	Min.	Typ	Max	Unit
Receiver						
Input threshold “H”		V_{THH}	10.5		13	V
Input threshold “L”		V_{THL}	8		11.5	V
Hystereisis		V_{HYS}	0	1		V
Input range CQ		V_{IN}	-10		VPLUS+ 10	V
Noise suppression time		t_{ND}		$1/(16.f_{BIT})$		µs
Data rate	BD=0	f_{BIT}		38.4		kBaud

Data rate	BD=1	f_{BIT}		230.4		kBaud
Bit time		T_{BIT}		1/ f_{BIT}		ms
Short circuit and Wake-up detection						
Set current		I_{SHORT}	-20%	190mA	+30%	mA
Filter display		t_{SHORT}	-10%	14	+10%	µs
Retries	SIO Mode	N_{RETRY}		2		
Retry delay	SIO Mode	t_{RETRY}	-10%	50	+10%	µs
Short circuit restart	SIO Mode	$t_{RESTART}$	-10%	100	+10%	ms
Regulator						
Power fail reverse leak		$I_{PLUSREV}$			10	µA
Regulator Output capability		I_{OUT}	50			mA
Startup static capability		R_{START_MIN}	67			Ω
Reg. output resistance		R_{OUT}		3		Ω
Regulator output voltage	10,0mA< I_{OUT}<50mA	V_{out}	3.0	3.3	3.6	V
Under-voltage detect	V_{UV}≥10V	V_{UV}	14.67	16.3	17.93	V
Line surge protection, parameters with respect to any pair CQ, VPLUS						
Protection leakage	V=±35V	I_{REVPOL}			10	µA
Protection threshold	I=0.5A	V_{PROT}	35	40	45	V

Table 6.1.3 Electrical parameters IO-Link

6.3 Electrical Parameters

Description	Symbol	Min.	Typ	Max	Unit
Supply voltage	V_{DD}	1.8	3.3	3.6	V
Supply current	I_{DD}	-	5.6	6.5	mA

Standard port pins configured as digital pins, RESET						
LOW-level input current	V_I = V; on-chip pull-up resistor disable	I_{IL}		0.5	10*	nA
HIGH-level input current	$V_I = V_{DD}$; on-chip pull-up resistor disable	I_{IH}		0.5	10*	nA
OFF-state output current	V_o = V; $V_o = V_{DD}$; on-chip pull-up/down resistor disable	I_{OZ}		0.5	10*	nA
Input Voltage	V_{DD} = 0	V_I	0		3.6	V
Output voltage	Output active	V_O	0		V_{DD}	V
LOW-level input voltage		V_{IL}			$0.3V_{DD}$	V
HIGH-level input voltage		V_{IH}	$0.7V_{DD}$			V
Hystereisis		V_{HYS}		0.4		V
HIGH-level output voltage	I_{OH} = 4 mA; 2.5 V ≤V_{DD}≤3.6V	V_{OH}	V_{DD}-0.4			V
	I_{OH} = 3 mA; 1.8 V ≤V_{DD}<2.5V	V_{OH}	V_{DD}-0.4			V
LOW-level output voltage	I_{OL} = 4 mA; 2.5 V ≤V_{DD}≤3.6V	V_{OL}			0.4	V
	I_{OL} = 3 mA; 1.8 V ≤V_{DD}<2.5V	V_{OL}			0.4	V
HIGH-level output current	V_{OH} = V – 0.4 V; 2.5 V ≤V_{DD}≤3.6V	I_{OH}	4			mA
	1.8 V ≤V_{DD}<2.5V	I_{OH}	3			mA
LOW-level output current	V_{OL} = 0.4 V;	I_{OL}	4			mA

	2.5 V ≤V_{DD}≤3.6V					
	1.8 V ≤V_{DD}<2.5V	I_{OH}	3			mA
HIGH-level short-circuit output current[3]	V_{OH} =0 V	I_{OHS}			45	mA
LOW-level short-circuit output current[3]	V_{OL} = V_{DD}	I_{OLS}			50	mA
Pull-up current	V_I =0 V; 2.0 V ≤V_{DD}≤3.6 V	I_{pu}	15	50	85	µA
	2.0 V ≤V_{DD}≤3.6 V	I_{pu}	10	50	85	µA

Table 6.2.3 Electrical parameters Analog and digital IO Group

Note:

1- Typical rating is not guaranteed. The values listed are for room temperature (25°C), nominal supply voltages.
2- Including voltage outputs in 3-state mode; 3-state outputs go into 3-state mode in Deep power-down mode
3- Allowed as long as the current limit does not exceed the maximum current allowed by device.
* Based on characterization. Not tested in production.

7 Dynamic characteristics

7.1 Power-up ramp conditions

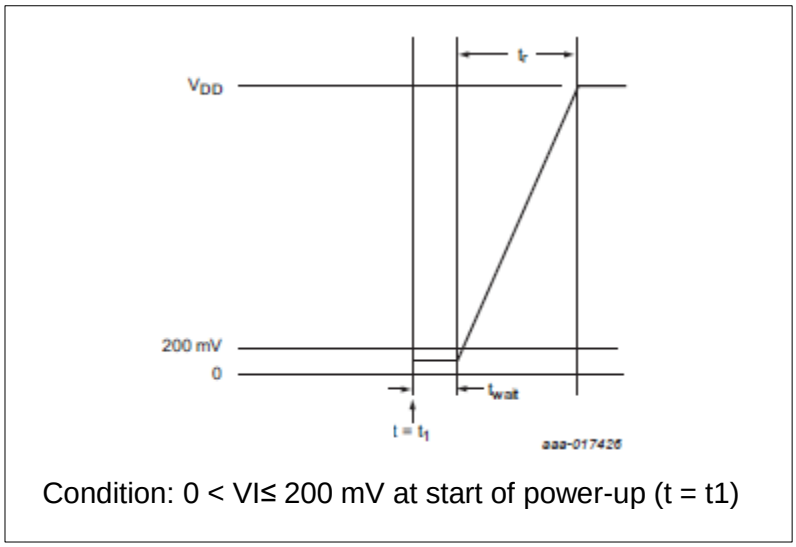
T_{amb} = -40 °C to +105 °C; 1.8 V ≤ VDD ≤ 3.6 V

Description	Condition	Symbol	Note	Min.	Typ	Max	Unit
rise time	at t = t_1: 0 < V_I≤ 200 mV	t_r	1, 3	0	-	500	ms
wait time		t_{wait}	1, 2	-	-	12	µs
input voltage	at t = t_1 on pin V_{DD}	V_I	3	0	-	200	mV

Table 7.1 Power-up characteristics

Note

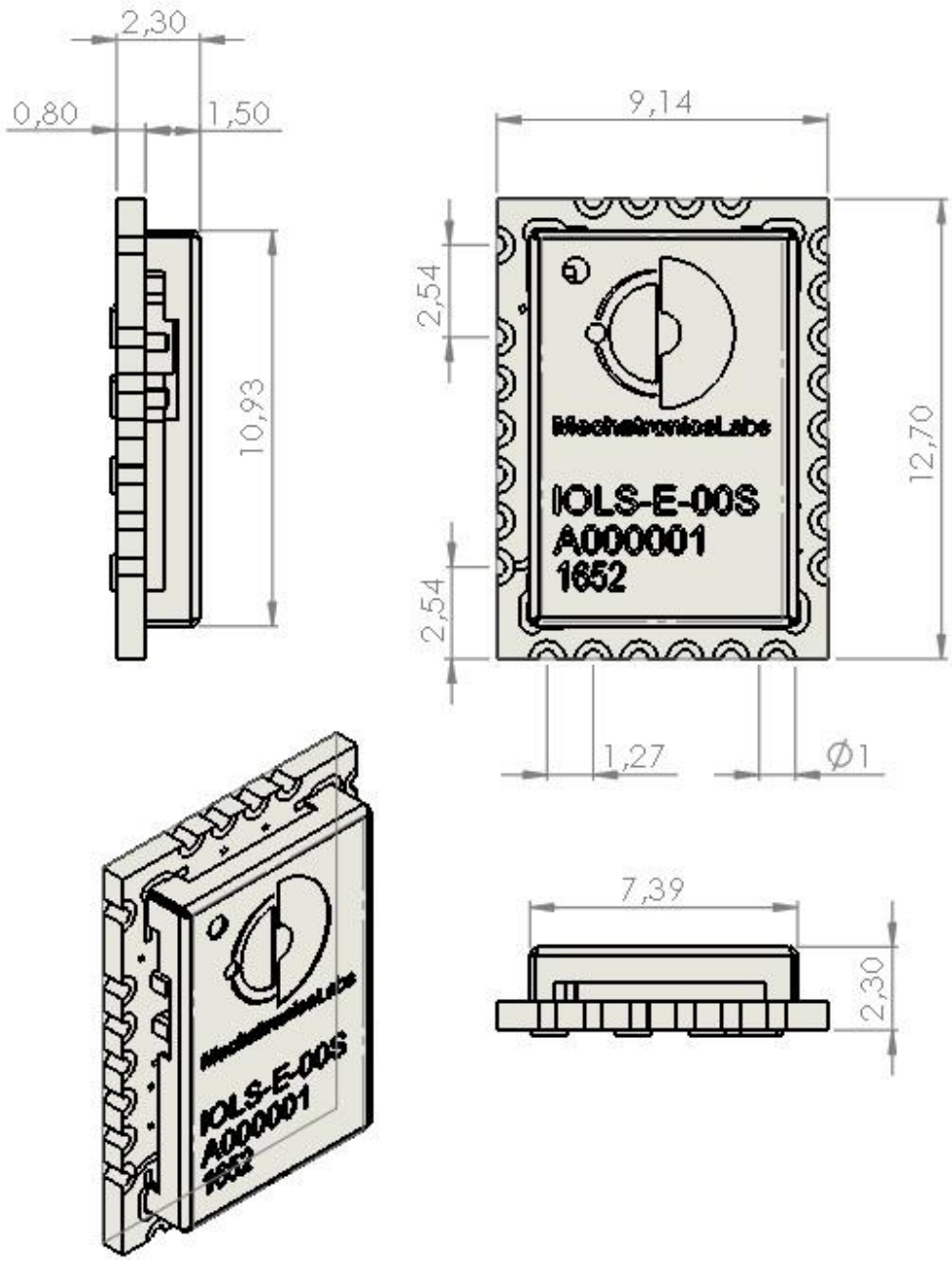
1- See Figure 6.1.
2- Based on simulation. The wait time specifies the time the power supply must be at levels below 200 mV before ramping up.
3- Based on characterization, not tested in production.



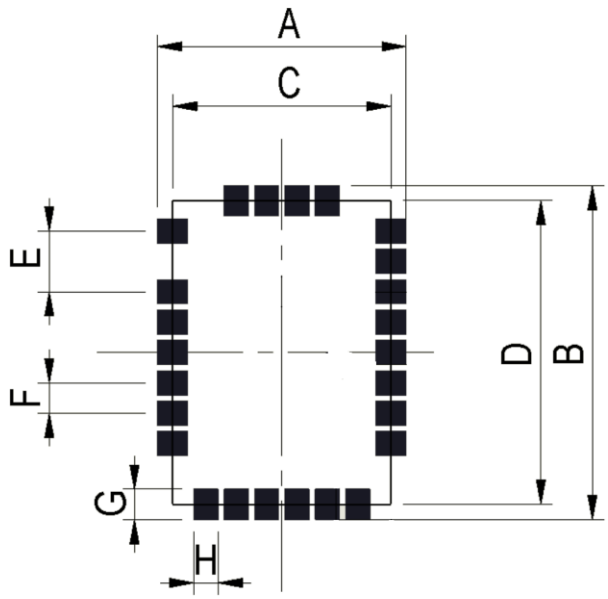
Condition: 0 < VI≤ 200 mV at start of power-up (t = t1)

Figure 7.1 Power-up rump

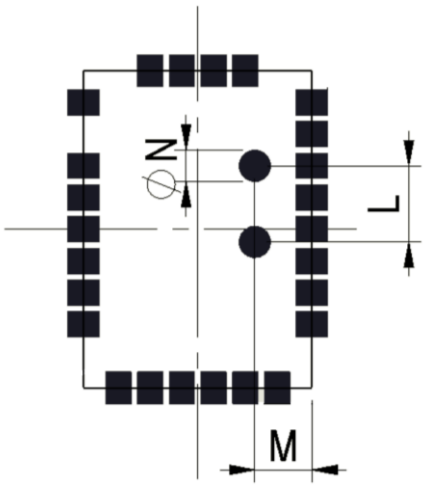
8 Mechanical



9 PCB Layout & Soldering



Typical layout footprint



Application mode/ developer layout footprint *

solder land

DIMENSIONS in millimeters and mils

	A	B	C	D	E	F	G	H	L*	M*	N*
mm	10,414	13,97	9,144	12,700	2,54	1,27	1,27	1,016	3,048	2,286	1,27
mils	410	550	360	500	100	50	50	40	120	90	50

*** Note**: Use this layout footprint only if the module IOLS-E is used in Application mode. Two pads added, are used for Serial Wire Debug connection. Refer to specific chapter for details.

9.1 Reflow Soldering Profile

Profile Feature	Symbol	Value (Pb-Free assembly)
Average ramp-up rate	T_{Smax} to T_p	3 °C/s maximum
Preheat Temperature minimum	T_{Smin}	150 °C
Preheat Temperature maximum	T_{Smax}	200 °C
Preheat Time	t_{Smin} to t_{Smax}	75 s
Time maintained above - Temperature	T_L	217 °C
Time maintained above - Time	t_L	70 s
Peak/classification temperature	T_p	260 °C
Time within 5 °C of actual peak temperature	t_p	35 s
Ramp-down rate	-	6 °C/s maximum
Time 25 °C to peak temperature	-	6 minutes maximum
Number of allowed reflow cycles	-	2

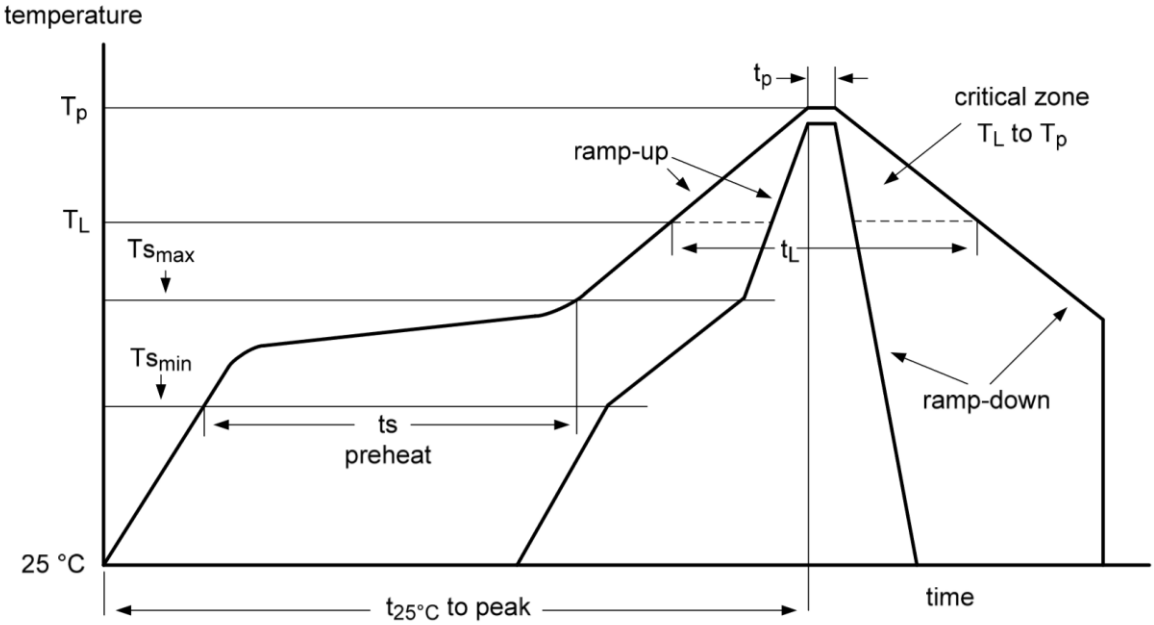
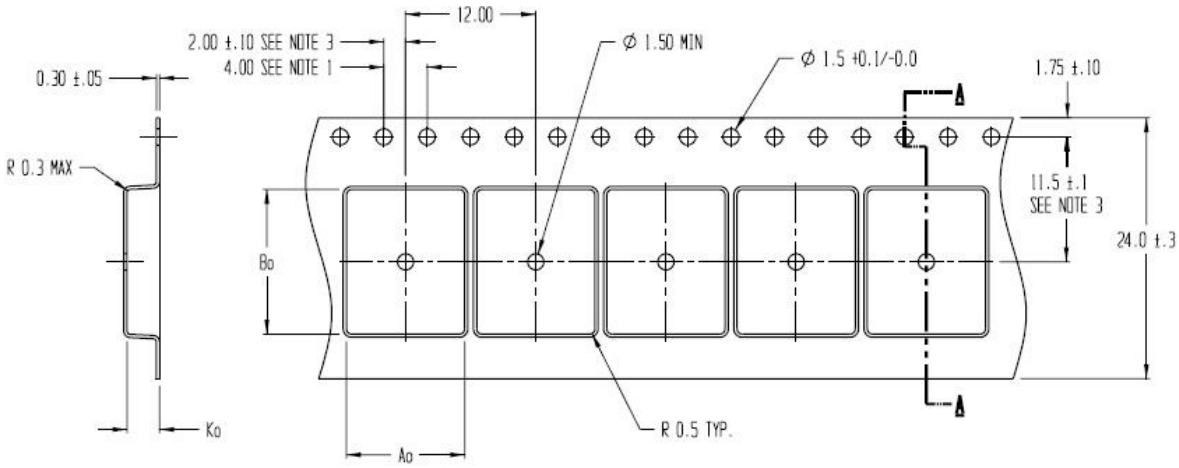


Figure 9.1.1 Reflow Soldering Profile

10 Packaging Reel



SECTION A - A

Ao = 10.90
Bo = 13.30
Ko = 3.00

NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

11 Revision History

Revision	Date	Chapter change	Change notice
1.0	17/05/2017	-	Release first document.
1.1	04/09/2018	3 4.3 4.4 4.6 5.1 5.2 9 4.8	Update pin-out and pin description. With BOOT, DAC and AVDD inserts. Minor fix on SS and RESET, added active low indication. Added debug pin for Application mode use. Added start-up configuration table Added timing diagram and characteristic mode for SPI communication in host mode. Added DAC pin and AVDD/REFP for analog unit. Added power ADC pin (AVDD) Completed Data model parameters description. Added Footprint for Application mode use and added reflow profile. Added chapter for brief description of the Application mode.

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